128MB (16M x 64) PC100 SDRAM MODULE

Features

- Intel PC SDRAM compalint 168 pins, dual in-line memory module (DIMM)
- Two memory rows on this module (Double Bank Module)
- Unbuffered DIMM
- Auto Refresh and Self Refresh
- CAS latency: 2 and 3
- Burst Length: 1, 2, 4, 8 and full page
- 4k refresh cycles/64ms
- Interface: LVTTL
- Serial Presence Detect with EEPROM
- Single 3.3V±0.3V power supply
- PCB: height (1,375 mil) single sided component

Part Number

Module Part Number	Speed Grade
W9828BADA-8H	PC100 CL=2
W9828BADA-8N	PC100 CL=3
W9828BADA-10	PC66 CL=2, 3

General Description

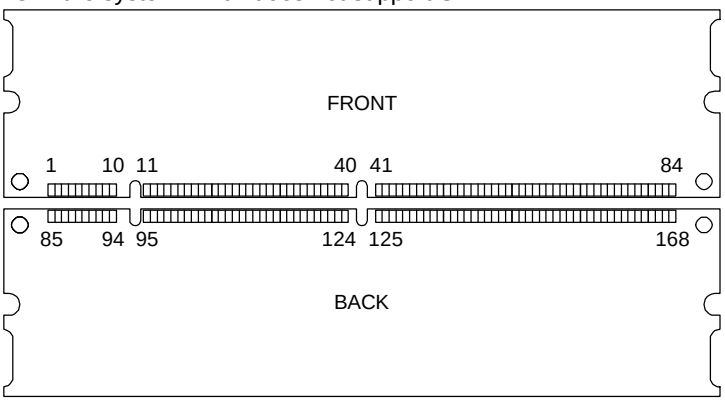
The Winbond W9828BADA is a 16M x 64 Synchronous Dynamic RAM memory module. This module consists of sixteen pieces of W986408AH (8M x 8 bit) SDRAMs in 54-pin TSOP-II 400mil package and a 2K EEPROM in 8-pin SOP package on a 168-pin 6-layer PCB. One 0.1 uF and one 0.33uF decoupling capacitor is used for each SDRAM.

The W9828BADA is a Dual In-line Memory Module for mounitng into 84-pin dual readout zigzag edge connector sockets. It is designed to operate in 3.3V memory systems.

Pin Assignment

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VSS	29	DQM1	57	DQ18	85	VSS	113	DQM5	141	DQ50
2	DQ0	30	CS0#	58	DQ19	86	DQ32	114	CS1#	142	DQ51
3	DQ1	31	NC	59	VDD	87	DQ33	115	RAS#	143	VDD
4	DQ2	32	VSS	60	DQ20	88	DQ34	116	VSS	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	NC	90	VDD	118	A3	146	NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	VSS	92	DQ37	120	A7	148	VSS
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	VSS	40	VDD	68	VSS	96	VSS	124	VDD	152	VSS
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	VSS	71	DQ26	99	DQ43	127	VSS	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2#	73	VDD	101	DQ45	129	CS3#	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	VDD	77	DQ31	105	*CB4	133	VDD	161	DQ63
22	*CB1	50	NC	78	VSS	106	*CB5	134	NC	162	VSS
23	VSS	51	NC	79	CLK2	107	VSS	135	NC	163	CLK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	**SA0
26	VDD	54	VSS	82	**SDA	110	VDD	138	VSS	166	**SA1
27	WE#	55	DQ16	83	**SCL	111	CAS#	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

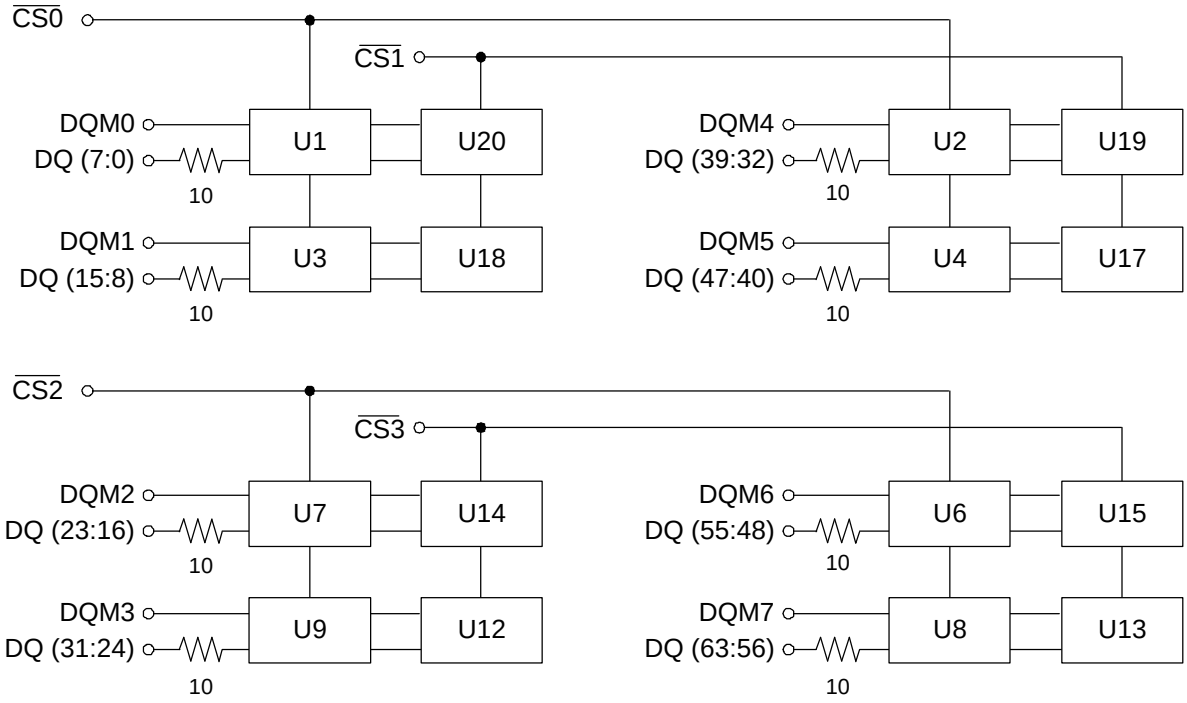
* These pins are not used in this module.
** These pins should be NC in the system which does not support SPD.

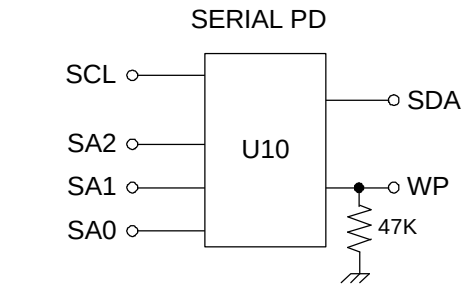


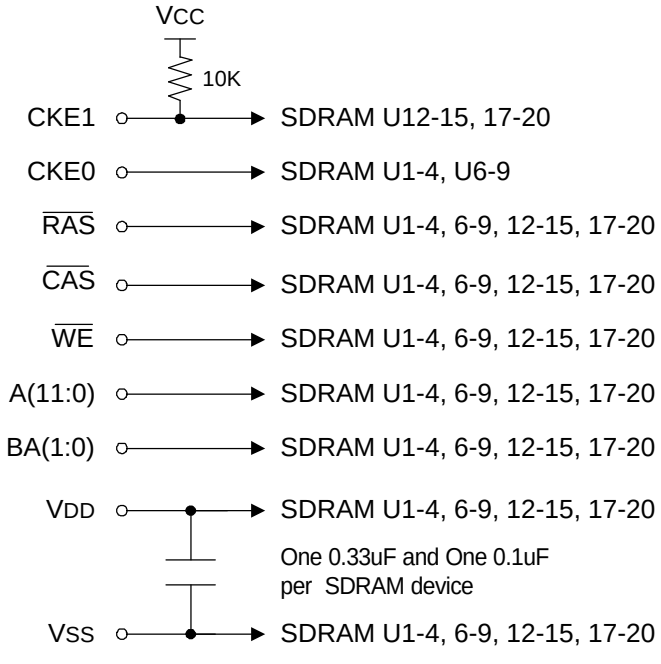
Pin Description

Pin	Name	Function Description
CLKn	Clock Inputs	System clock used to sample inputs on the rising edge of clock.
CSn#	Chip select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
CKEn	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self-Refresh mode is entered.
A0~A11	Address	Multiplexed pins for row and column address. Row address: A0~A11. Column address: A0~A8.
BA0~BA1	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
RAS#	Row Address Strobe	Command input. When sampled at the rising edge of the clock, RAS#, CAS# and WE# define the operation to be executed.
CAS#	Column Address Strobe	Referred to RAS#
WE#	Write Enable	Referred to RAS#
DQM0~7	Input/Output Mask	The output buffer is placed at Hi-Z when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write data.
DQ0~63	Data Input/Output	Multiplexed pins for data output and input
V_{DD}	Power (+3.3 V)	Power for input buffers and logic circuit inside SDRAM.
V_{SS}	Ground	Ground for input buffers and logic circuit inside SDRAM.
SCL	Serial Clock	Clock for serial presence detection
SDA	Serial Data I/O	Data line for serial presence detection
SAn	SPD Address Line	System assigned address (SA0~SA2) to identify different memory module in a system board.
NC	No Connection	No connection

BLOCK DIAGRAM







CLOCK WIRING	
CLOCK INPUT	LOAD
CLK0	4 SDRAMS + 3.3pF cap
CLK1	4 SDRAMS + 3.3pF cap
CLK2	4 SDRAMS + 3.3pF cap
CLK3	4 SDRAMS + 3.3pF cap

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}, V_{OUT}	Input, column Output Voltage	-0.3~V_{CC}+0.3	V	
V_{DD}	Power Supply Voltage	-0.3~4.6	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	-55~125	°C	
P_D	Power Dissipation	18	W	
I_{OUT}	Short Circuit Output Current	50	mA	

Note: Operation exceeds "ABSOLUTE MAXIMUM RATING" may cause permanent damage to the devices.

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V	
V_{IH}	Input High Voltage	2.0	-	V_{CC}+0.3	V	
V_{IL}	Input Low Voltage	-0.3	-	0.8	V	

Note: V_{IH}(max) = V_{DD} +1.2V for pulse width $\leq$ 5ns
V_{IL}(min) = V_{SS} -1.2V for pulse width $\leq$ 5ns
All voltages are referenced to V_{SS}

CAPACITANCE (VCC=3.3V, Af = 1MHz, Ta=25°C)

PIN	SYMBOL	MIN	MAX	UNIT
Address(A0~A11, BA0~BA1)	Cadd	-	64	pf
RAS#, CAS#, 1WE#	Ccmd	-	64	pf
CKE0, CKE1	C_{CKE}	-	32	pf
CLK0, CLK1, CLK2, CLK3	C_{CLE}		27.3	pf
CS0#, CS1#, CS2#, CS3#	C_{CS}	-	16	pf
DQM0~DQM7	C_{DQM}	-	8	pf
DQ0~DQ63	C_{IO}	-	10	pf

DC CHARACTERISTICS

(VCC = 3.3V ± 0.3V, Ta=0°~70°C)

SYMBOL	ITEMS		-8H/-8N		-10		UNIT	NOTES
			MIN	MAX	MIN	MAX		
I_{CC1}	OPERATING CURRENT (t_{CK}=min, t_{RC}=min) Active Precharge command cycling without burst operation	1 Bank Operation		1520		1280	mA	1, 3
I_{CC2}	STANDBY CURRENT (t_{CK}=min, CS#=V_{IH} $V_{IH/L}$=$V_{IH(min)}$/$V_{IL(max)}$ Bank: inactive state)	CKE=V_{IH}		960		800	mA	1
I_{CC2P}		CKE=V_{IL} (Power Down mode)		48		48		
I_{CC2S}	STANDBY CURRENT (CLK=V_{IL}, CS#=V_{IH} $V_{IH/L}$=V_{IH}(min)/V_{IL}(max) BANK: inactive state)	CKE=V_{IH}		80		80	mA	
I_{CC2PS}		CKE=V_{IL} (Power Down mode)		32		32		
I_{CC3}	NO OPERATING CURRENT (t_{CK}=min, CS#=V_{IH}(min) BANK: active state (4 banks))	CKE=V_{IH}		1200		960	mA	1, 3
I_{CC3P}		CKE=V_{IL} (Power Down mode)		128		128	mA	1
I_{CC4}	BURST OPERATING CURRENT (t_{CK}=min, CS#=V_{IH}(min), Read/Write command cycling)			2160		1920	mA	1, 2, 3
I_{CC5}	AUTO REFRESH CURRENT (t_{CK}=min, t_{RC}=min, Auto Refresh command cycling			1680		1440	mA	1, 3
I_{CC6}	SELF REFRESH CURRENT (Self Refresh mode CKE=0.2V)			32		32	mA	

Note: 1. These parameters depend on the cycle rate and listed values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.

2. These parameters depend on the output loading. The specified values are obtained with output open

3. These valuse are measured under the following conditions
   Front(or back): Under the measuring conditions given on the data sheet
   Back(or front): In stand by (measured under the $I_{CC}2$ conditions)

AC CHARACTERISTICS AND OPERATING CONDITION

(Vcc=3.3V±0.3V, Ta=0° to 70°C)

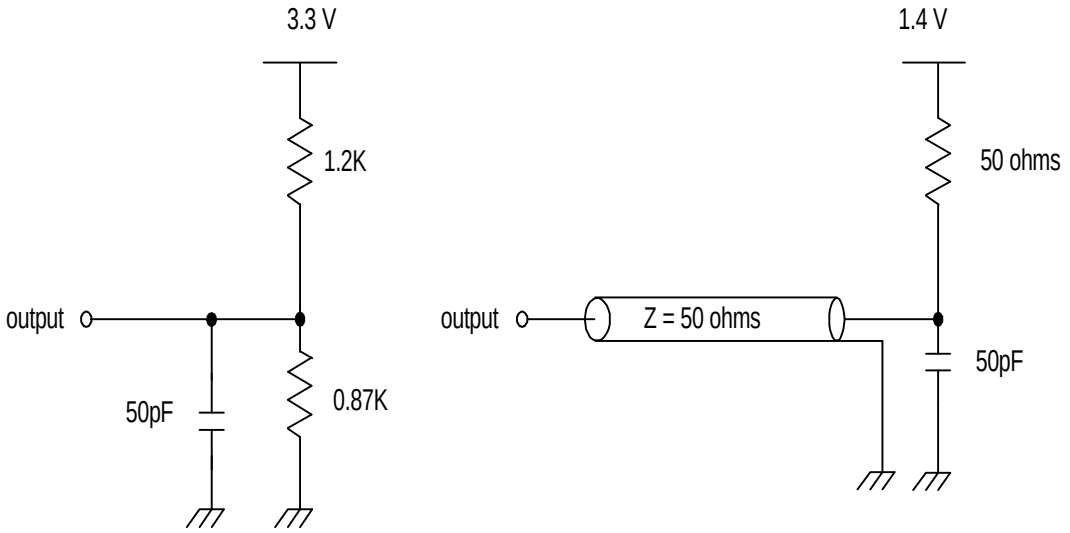
SYMBOL	PARAMETER		-8H		-8N		-10		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Ref/Active to Ref/Active Command Period		68		72		90		ns
t_{RAS}	Active to precharge Command Period		48	100000	48	100000	60	100000	
t_{RCD}	Active to Read/Write Command Delay Time		20		20		30		
t_{CCD}	Read/Write(a) to Read/Write(b)Command Period		1		1		1		cycle
t_{RP}	Precharge to Active Command Period		20		20		30		ns
t_{RRD}	Active(a) to Active(b) Command Period		20		20		20		
t_{WR}	Write Recovery Time	CL*=2	10		12		15		
		CL*=3	8		10		10		
t_{CK}	CLK Cycle Time	CL*=2	10		12	1000	15	1000	
		CL*=3	8		10	1000	10	1000	
t_{CH}	CLK High Level		3		3		3		
t_{CL}	CLK Low Level		3		3		3		
t_{AC}	Access Time from CLK	CL*=2		6		7		9	
		CL*=3		6		6		8	
t_{OH}	Output Data Hold Time		3		3		3		
t_{HZ}**	Output Data High Impedance Time		3	8	3	8	3	10	
t_{LZ}	Output Data Low Impedance Time		0		0		0		
t_{SB}	Power Down Mode Entry Time		0	8	0	8	0	10	
t_{T}	Transition Time of CLK (Rise and Fall)		0.5	10	0.5	10	0.5	10	
t_{DS}	Data-in-Set-up Time		2		2		3		
t_{DH}	Data-in Hold Time		1		1		1		
t_{AS}	Address Set-up Time		2		2		3		
t_{AH}	Address Hold Time		1		1		1		
t_{CKS}	CKE Set-up Time		2		2		3		
t_{CKH}	CKE Hold Time		1		1		1		
t_{CMS}	Command Set-up Time		2		2		3		
t_{CMH}	Command Hold Time		1		1		1		
t_{REF}	Refresh Time			64		64		64	ms
t_{RSC}	Mode register Set Cycle Time		16		16		20		ns

Note: *CL= CAS Latency

** t_{HZ} defines the time at which the outputs achieve the open circuit condition and is not referenced to output level. Refer to the individual component

AC TESTING CONDITIONS

Output Timing Measurement Reference Level	1.4V/1.4V
Output Load	See diagram B Below
Input Signal Levels	2.4V/0.4V
Transition Time (Rise and Fall) of Input Signal	2ns
Input Reference Level	1.4V



AC TEST LOAD (A)

AC TEST LOAD (B)

Note: Transition times are measured between V_{IH} and V_{IL}.

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 1 shows the truth table for the operation commands.

Table 1: Truth Table (note (1), (2))

COMMAND	Device state	CKEn-1	CKEn	DQM	BA0, BA1	A10	A11, A9-0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Bank Active	Idle	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active (3)	H	X	X	V	L	V	L	H	L	L
Write with Autoprecharge	Active (3)	H	X	X	V	H	V	L	H	L	L
Read	Active (3)	H	X	X	V	L	V	L	H	L	H
Read with Autoprecharge	Active (3)	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No–Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active (4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto–Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self-Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	idle (S.R.)	L L	H H	X X	X X	X X	X X	H L	X H	X H	X X
Clock suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Idle Active (5)	H H	L L	X X	X X	X X	X X	H L	X H	X H	X X
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (power down)	L L	H H	X X	X X	X X	X X	H L	X H	X H	X X
Data write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Notes: (1) V=Valid X=Don't care L=Low Level H=High Level
(2) CKEn signal is input level when commands are provided.
(3) These are state of bank designated by BA0, BA1 signals.
(4) Device state is full page burst operation.
(5) Power Down Mode can not be entered in the burst cycle. When this command asserts in the burst cycle, device state is clock suspend mode

Serial Presence Detect EEPROM

The Serial Presence Detect (SPD) function is implemented using a 2,408-bit EEPROM component. This nonvolatile storage device contains data for identifying the module type and various SDRAM organization and timing parameters. System read operations to the EEPROM device occur using the DIMM SCL(clock) and SDA (data) signals, together with SA(2:0) which provide the EEPROM Device Address.

SPD EEPROM DC OPERATING CONDITIONS

(Vcc=3.3V±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNIT	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	V_{CC}×.7	V_{CC}+ .5	V	
Input Low (logic 0) Voltage, all inputs	V_{IL}	-0.3	V_{CC}×.3	V	
OUTPUT LOW VOTAGE, Iout=3 Ma	V_{OL}		0.4	V	I_{OL}=3mA
INPUT LEAKGE CURRENT, Vin =GND to Vcc	I_{LI}		1	uA	
OUTPUT LEAKAGE CURRENT, V_{OUT}=GND to Vcc	I_{LO}		1	uA	
STANDBY CURRENT SCL=SDA Vcc-0.3V, All other inputs=GND or 3.3V +10%	I_{SB}		10	uA	
POWER SUPPLY CURRENT SCL clock frequency = 100KHz	I_{CC}		1	mA	

SPD AC OPERATING CONDITIONS

(Vcc=3.3V±0.3V)

AC CHRARCTERICS					
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNIT**	**NOTES**
SCL clock frequency	f_{SCL}		100	KHz	
Noise Suppression Time Constant at SCL,SDA Inputs	t_I		100	ns	
SCL Low to SDA Data Out Valid	t_{AA}	0.3	3.5	us	
Time the bus must be free before a new transition can start	t_{BUF}	4.7		us	
Start Condition Hold Time	$t_{HD:STA}$	4.0		us	
Clock Low Period	t_{LOW}	4.7		us	
Clock High Period	t_{HIGH}	4.0		us	
Start Condition Setup Time	$t_{SU:STA}$	4.7		us	
Data in Hold Time	$t_{HD:DAT}$	0		us	
Data in Setup Time	$t_{SU:DAT}$	250		ns	
SDA and SCL Rise time	t_R		1	us	
SDA and SCL Fall Time	t_F		300	ns	
Stop Condition Setup Time	$t_{SU:STO}$	4.7		us	
Data Out Hold Time	t_{DH}	300		ns	
Write Cycle Time	t_{WR}		15	ms	

Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle the EEPROM bus interface circuits are disabled, SDA is allowed to remain high the bus level pull-up resistor, and the device does not respond to its slave address.

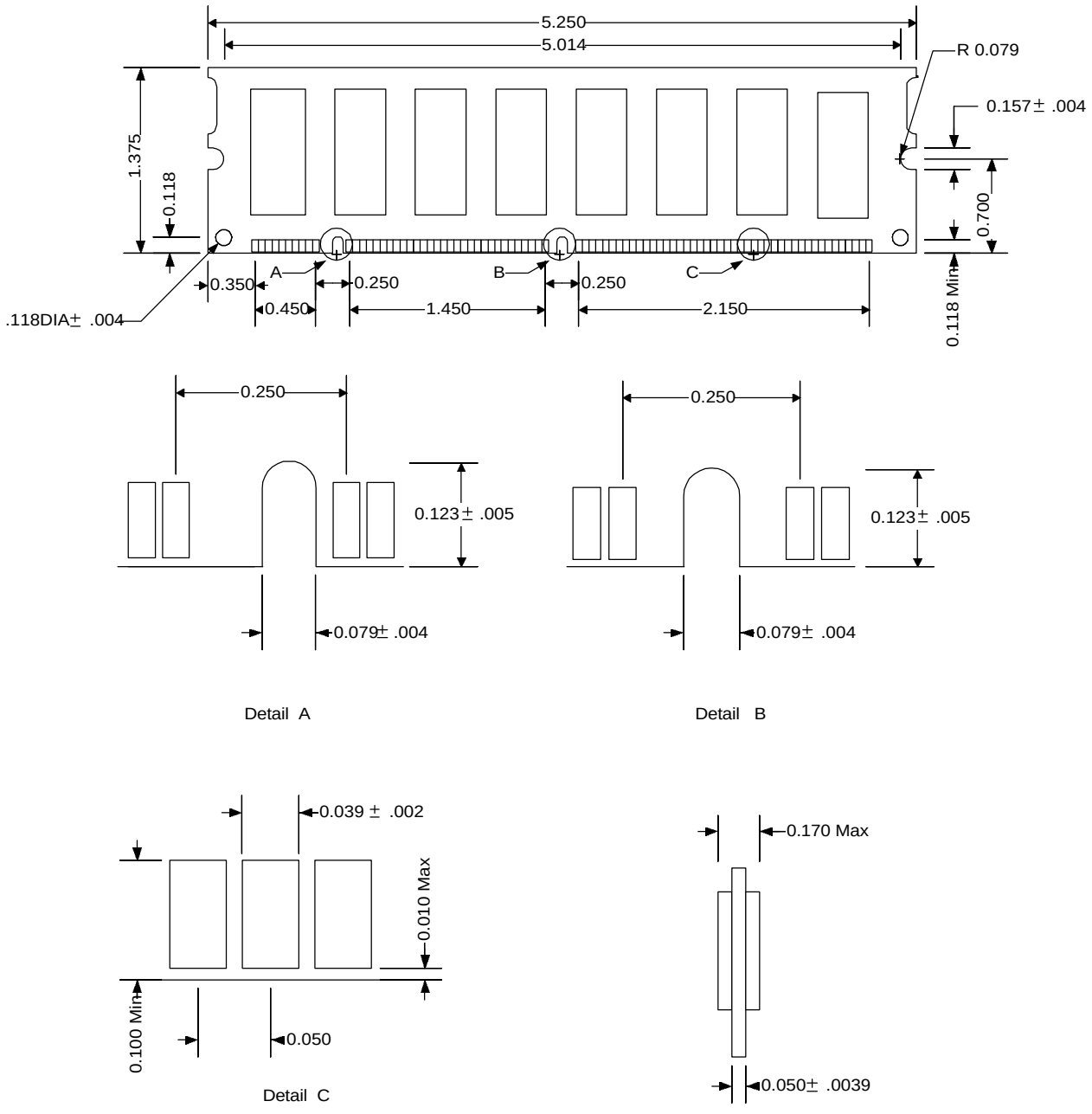
CONTENTS OF EEPROM (SPD Versions 1.2)

Byte Number	FUNCTION DESCRIBED	FUNCTION SUPPORTED			HEX VALUE		
		-8H	-8N	-10	-8H	-8N	-10
0	Defines # bytes written into serial memory at module manufacturer	128 bytes			80h		
1	Total # bytes of SPD memory device	256 bytes (2K- bit)			08h		
2	Fundamental memory type (FPM, EDO, SDRAM..)	SDRAM			04h		
3	# Row Addresses on this assembly	12			0Ch		
4	# Column Addresses on this assembly	9			09h		
5	# Module Rows on this assembly	2 row			02h		
6	Data Width of this assembly..	64 bits			40h		
7	..Data Width continuation	-			00h		
8	Voltage interface standard of this assembly	LVTTL			01h		
9	SDRAM Cycle time @CAS latency of 3	8ns	10ns	10ns	80h	A0h	A0h
10	SDRAM Access time form clock @CAS latency of 3	6ns	6ns	8ns	60h	60h	80h
11	DIMM Configuration type (Non-parity, Parity ECC)	Non parity			00h		
12	Refresh Rate/Type	15.625 us, support self refresh			80h		
13	SDRAM width , Primary DRAM	X8			08h		
14	Error Checking SDRAM data width	None			00h		
15	Minimum Clock Delay, Back Random Column Addresses	TCCD =1 CLK			01h		
16	Burst Lengths supported	1, 2, 4, 8 & full page			8Fh		
17	#Bank on Each SDRAM device	4 banks			04h		
18	CAS# Latencies Supported	2 & 3			06h		
19	CS# Latency	0 CLK			01h		
20	Write Latency	0 CLK			01h		
21	SDRAM Module Attributes	Non-buffered Non –registered & redundant addressing			00h		
22	SDRAM Device Attributes: General	+/-10% voltage tolerance , Burst Read, Single bit Write, precharge all, auto precharge			0Eh		
23	SDRAM cycle time @CAS latency of 2	10ns	12ns	15ns	A0h	C0h	F0h
24	SDRAM access time form clock @CAS latency of 2	6ns	6ns	9ns	60h	60h	90h
25	SDRAM cycle time @CAS latency of 1	-	-	-	00h	00h	00h
26	SDRAM access time from clock @CAS latency of 1	-	-	-	00h	00h	00h
27	Precharge to active command period (t_{RP})	20ns	20ns	30ns	14h	14h	1Eh
28	Active to Active command period (t_{RRD})	20ns	20ns	20ns	14h	14h	14h
29	Active to Read/Write command delay time(t_{RCD})	20ns	20ns	30ns	14h	14h	1Eh
30	Minimum Active to precharge period (t_{RAS})	48ns	48ns	60ns	30h	30h	3Ch
31	Density of each Row on Module	2 row of 64MB .			10h		
32	Command and Address signal input setup time	2ns	2ns	3ns	20h	20h	30h
33	Command and Address signal input hold time	1ns			10h		
34	Data signal input setup time	2ns	2ns	3ns	20h	20h	30h
35	Data signal input hold time	1ns			10h		
36-61	Superset Information(may be used in future)	-			00h		
62	SPD Revision	Current release Intel spd 1.2			12h		
63	Checksum for Bytes 0-62	-			E4h	24h	E4h
64-71	Manufacturers code				MFG Dep		
72	Manufacturing location				MFG Dep		
73-90	Manufacturer's Part Number				MFG Dep		
91-92	Revision Code				MFG Dep		
93-94	Manufacturing Date				MFG Dep		
95-98	Assembly Serial Number				MFG Dep		
99-125	Manufacturer Specific Data				MFG Dep		
126	System frequency for 100 MHz	100MHz		66MHz	64h		66h
127	Intel Specification details	Detailed 100MHz Information			F7h	F5h	06h
128+	Unused storage locations				FFh		

128MB (16M x 64) PC100 SDRAM MODULE

PACKGE DIMENSIONS

Units:Inches



Tolerances: ± .005 unlesss othrerwise specified
The used device is 8M*8 SDRAM,TSOP